650 MHz SSPA control and Interface

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(On behalf of team RFSD)

PIP-II Technical Workshop

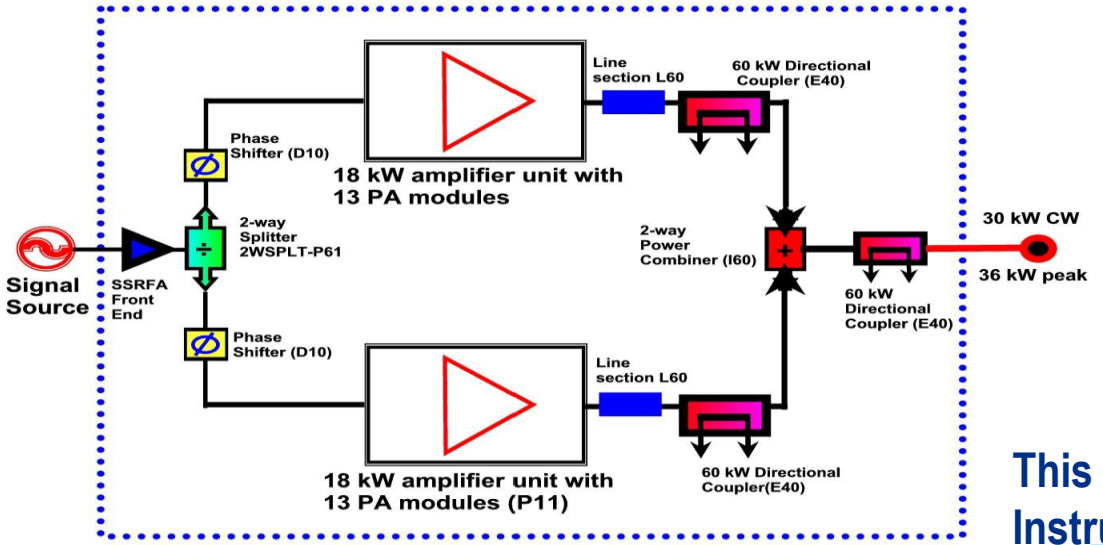
A Partnership of:

US/DOE
India/DAE
Italy/INFN
UK/UKRI-STFC
France/CEA, CNRS/IN2P3
Poland/WUST

Design and Development of 650 MHz CW solid state RF amplifier

- 650 MHz Solid State RF Amplifier designed as per TRS finalized under IIFC collaboration was developed
- It has two custom designed amplifier cabinets of 18 kW each RF power combines with high power two way combiner
- 99 numbers of 500 W RF amplifier modules along with DC power supply modules, control/interlock cards, directional sensors, 48 port dividers & 48 port combiner and 40 kW two way combiner.
- Tested at full power at 650 MHz with 50 ohms water cooled dummy load.

PARAMETER	Value
RF output power	36 kW CW
Bandwidth @ 1 dB	±2 MHz
Power gain	> 85 dB
Bias voltage	48 V DC
Harmonics response	-30 dBc Max, tested within 2 GHz bandwidth
Spurious response	-50 dBc Max including power supply modulation, tested within 2 GHz bandwidth
AC input	3 phase 440V, 50 Hz
Physical dimensions	4.4 m x 2.2 m x 2 m (H)

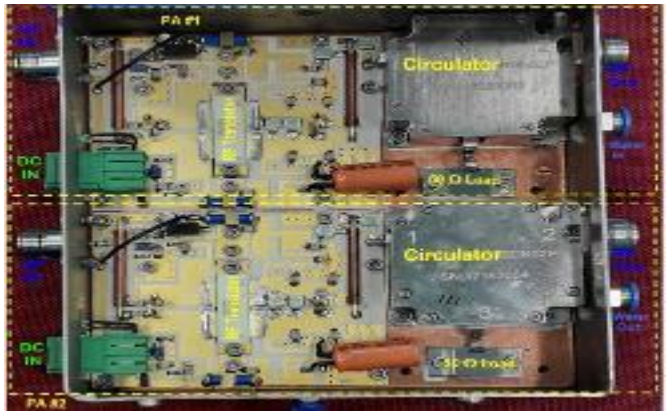


This work was submitted recently in Rev of Scientific Instruments Journal.

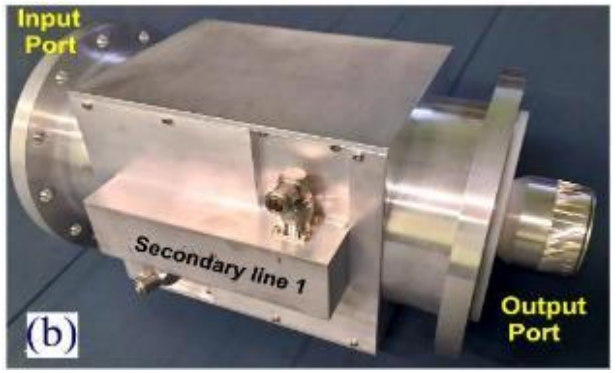
PIP-II

Main RF Components of 650 MHz Solid State RF Amplifier

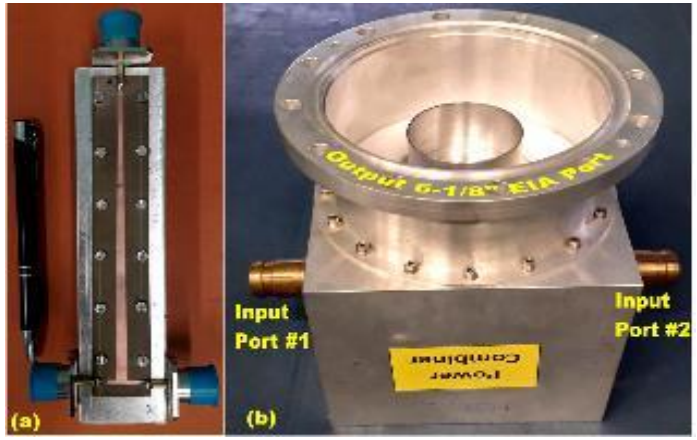
1. **Rigid Coaxial RF Components** Directional couplers, divider, combiner, mounting hardware etc. -1 set
2. **Power Amplifier (PA) Module** with water cooled enclosures, RF components and RF connectors (one PA module consists of four gain block) – 26 sets
3. **Amplifier Cabinet/Unit** wired and assembled with 3 phase electrical system, DC bias supplies, water headers, water tubes, PT 100 temperature measurement hardware, front panel hardware – 2 sets
4. **Embedded SSRFA control subsystem** including FPGA Controller, digital, analog input, output modules, RF Detectors, Industrial PC, directional sensors etc. – 2 sets



2 kW (4X500W) PA assembly



Directional coupler with 6-⅛″ ports

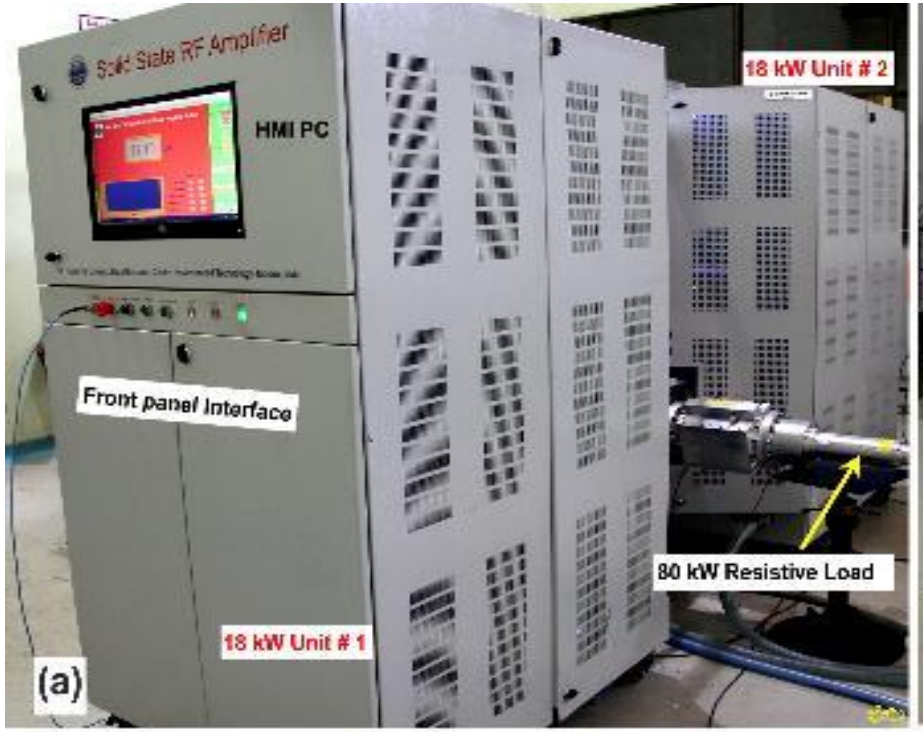


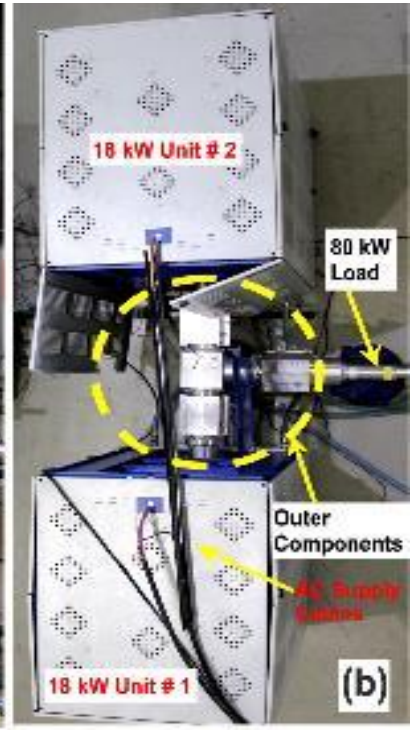
Fabricated 2-port (a) tapered microstrip divider (b) High power combiner with 6-⅛″ input and output ports.

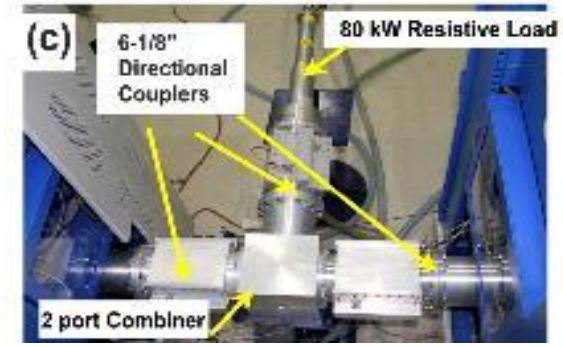
RF Power Sensor

Four of these developed technologies have been suitably transferred to private vendor through TTCD BARC.

650 MHz Solid State RF Amplifier







Control System Scheme

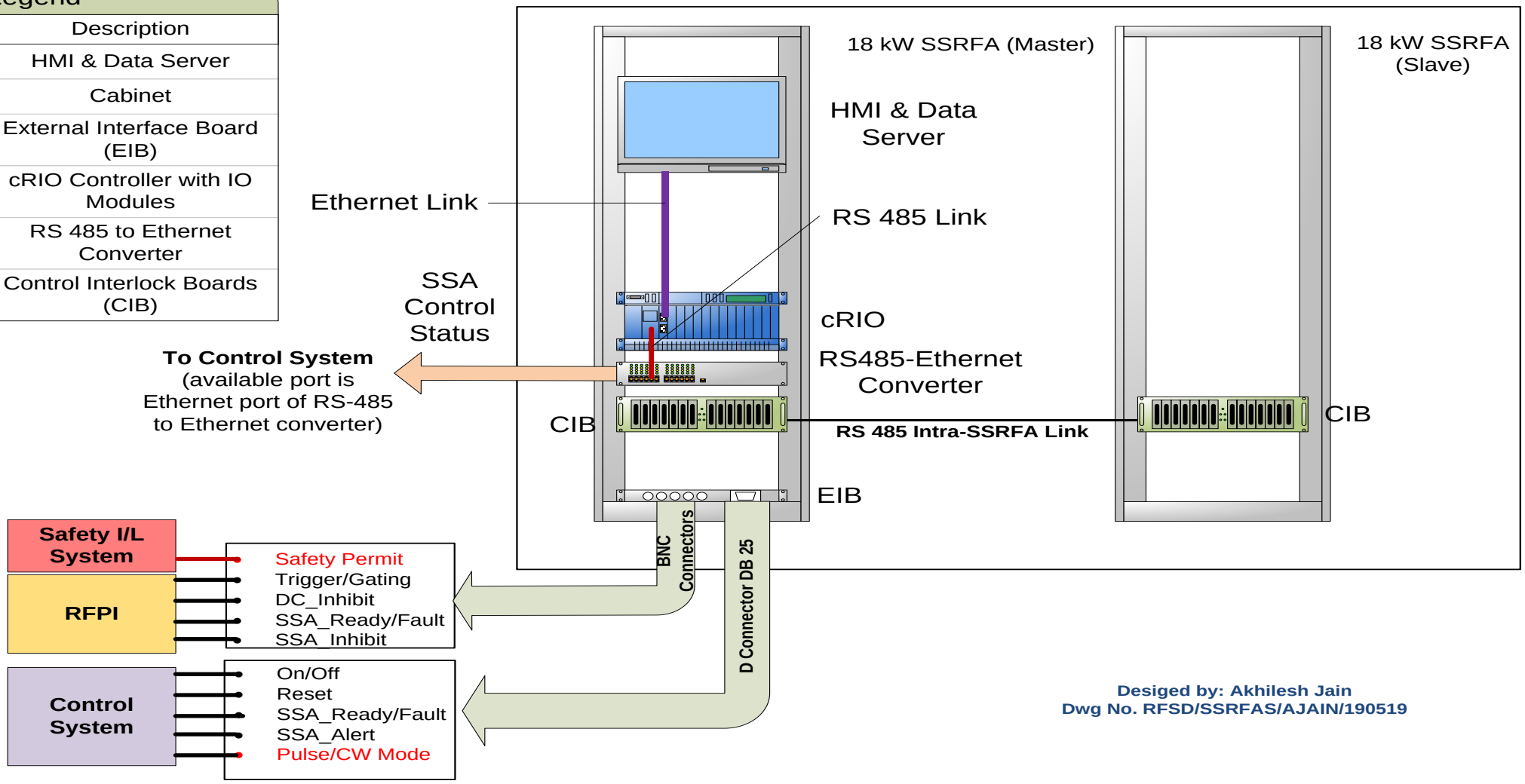
For data acquisition, each 18 kW unit together with its interlocks form an self contained system with its own embedded control operations performed by a graphical code developed in-house using LabVIEW™ RT and FPGA.

All of the PAs, with the help of 1 kW coupler provide rectified sample of forward and reflected power to cRIO controller (from National Instruments™) through RS485 networks connected on its 4-port module.

The whole system works as a distributed system over TCP/IP network where two 18 kW units function as master and slave respectively, and they are centrally coordinated by a master controller and interfaced with a PC running a LabVIEW based HMI application.

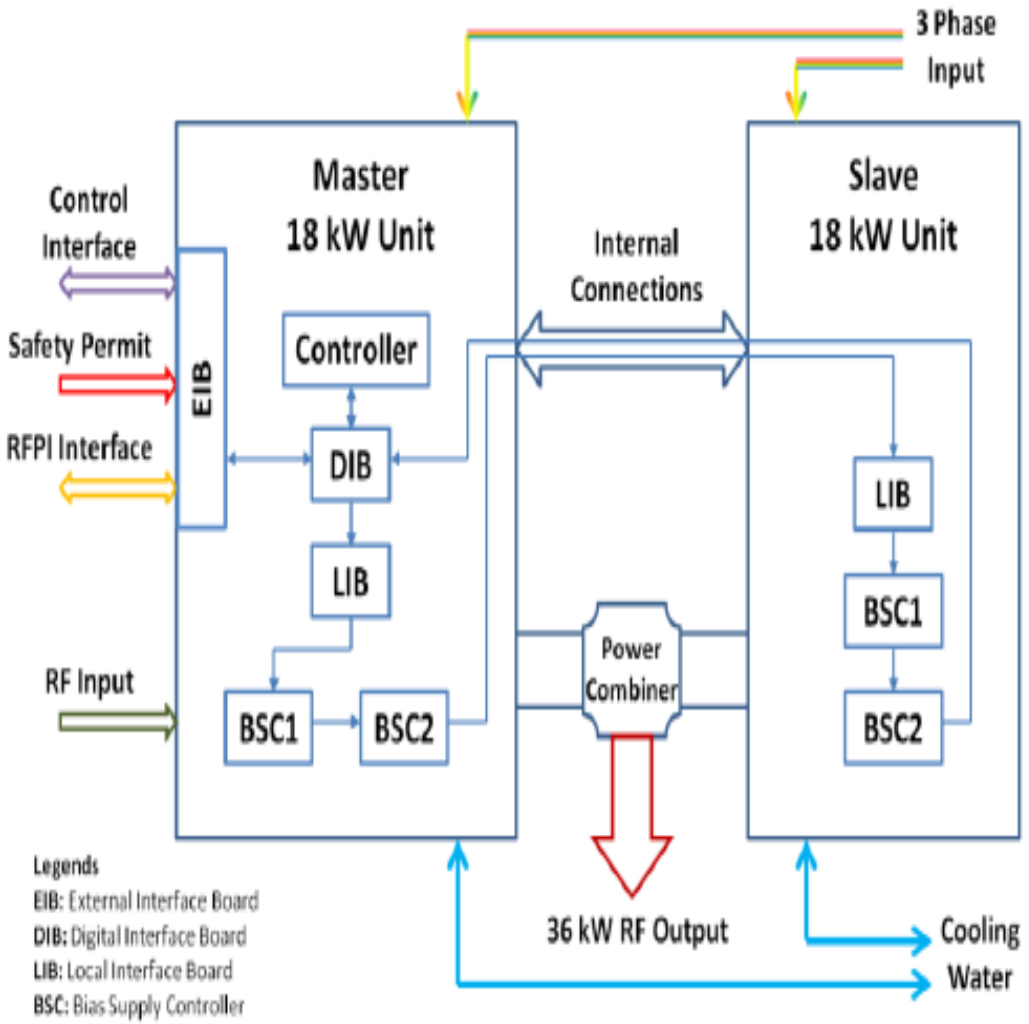
Designed Control/Interlock Scheme for 650 MHz SSRFA

Legend		
Symbol	Count	Description
	1	HMI & Data Server
	2	Cabinet
	1	External Interface Board (EIB)
	1	cRIO Controller with IO Modules
	1	RS 485 to Ethernet Converter
	2	Control Interlock Boards (CIB)



Low power amplifier and control/interlock hardware is different in both units, all other details are same for both master and slave units.

Different Control Interface Boards

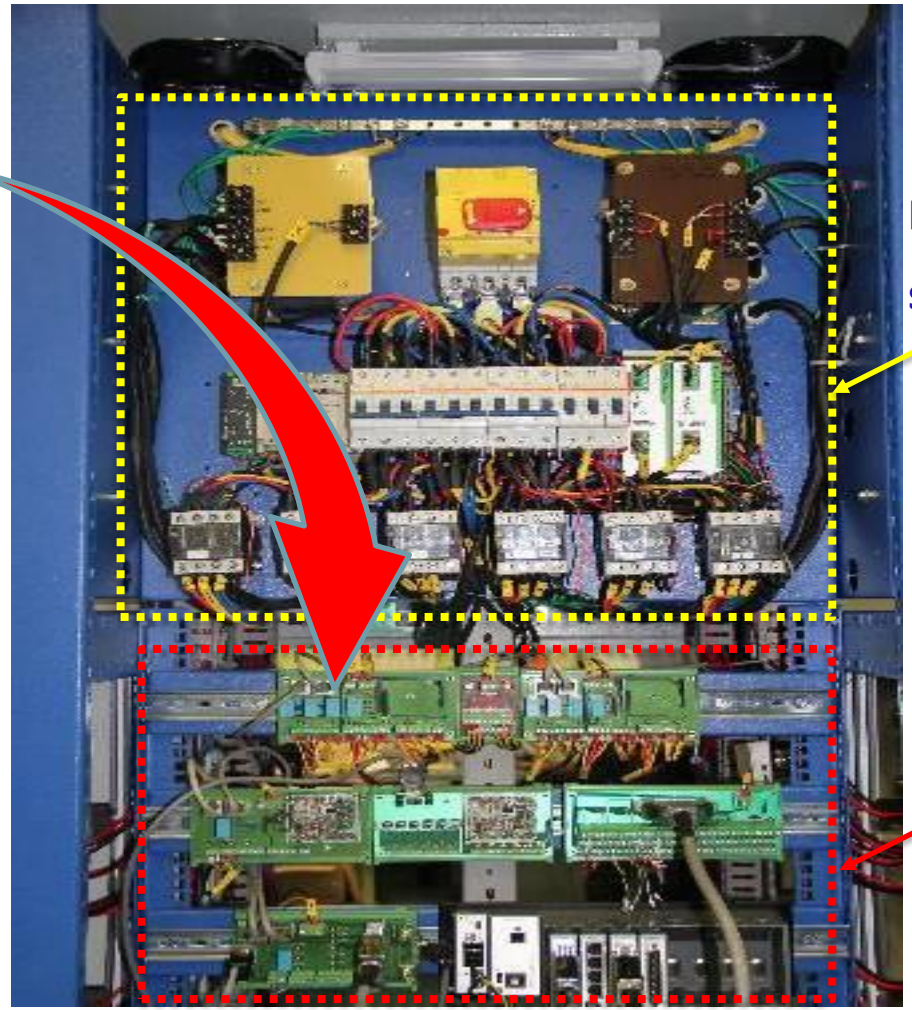


Sr. No.	Name	Function
1	Local Interface board (LIB)	It accepts all control/interlock signals of the rack/unit.
2	External interface board (EIB)	It is responsible for external/remote communication on RS 485 bus. It is part of only master unit.
3	Bias Supply Controller (BSC)	It controls ON/OFF sequence of 3 phase contactor.
4	Microcontroller unit (MCU)	It is core unit of all control/interlock boards except Digital interface board and Temperature input board.
5	Front panel controller (FPC)	It is local human interface for complete unit.
6	Digital interface board (DIB)	It is interface between input/output signals from of the cRIO controller. It also communicates with FPC. It does not have embedded Microcontroller unit.

For data acquisition, each 650 MHz unit is equipped with Control Interface Boards. Embedded control operations are performed by a graphical code developed in-house using LabVIEW™ RT and FPGA.

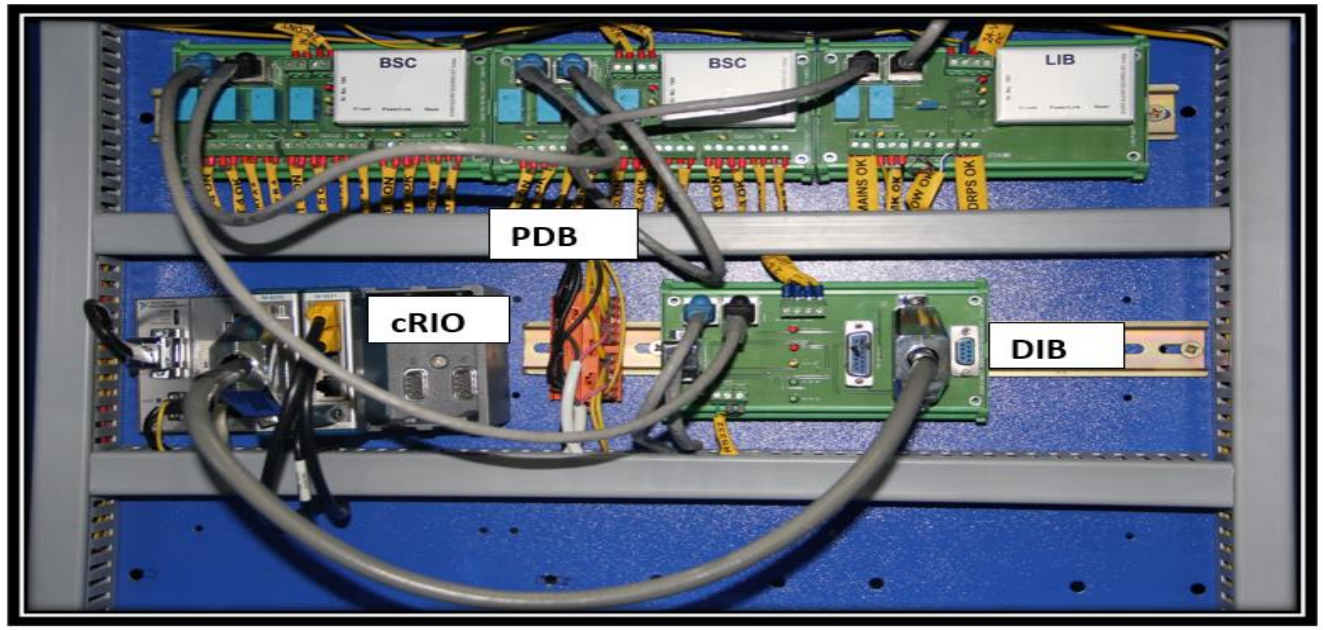
Embedded SSRFA Control Sub-system

Rear view of 18 kW amplifier Unit



Electrical section & Control/Interlock subsystem

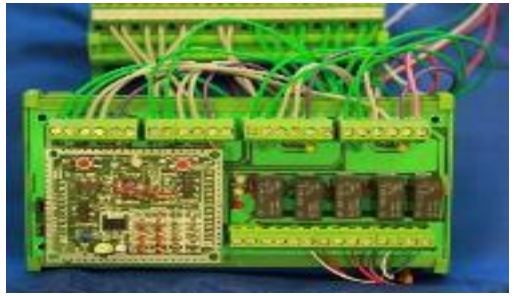
Few Control Interface Boards



Typical CIB Connections

Front Panel Controller

Temperature Sensor Interface Board

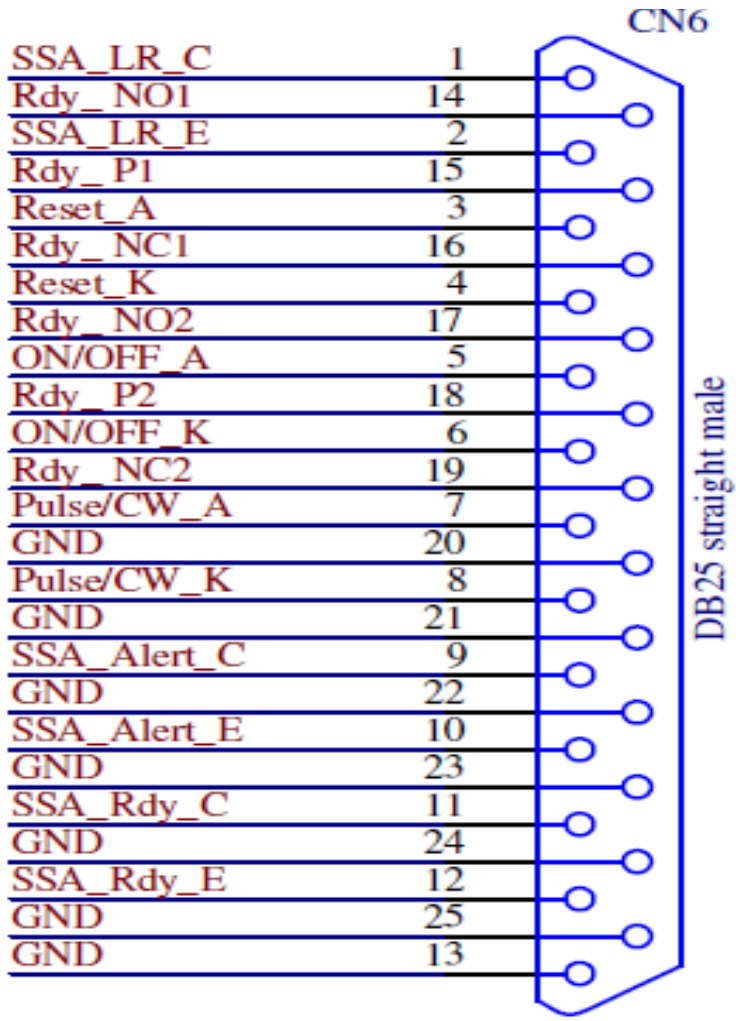


Bias Supply Controller

Amplifier Interface Signals..

ON/OFF (Start/OFF): This signal is required to soft start amplifier. This signal is generated external to SSRFA either by control system during Remote mode or manually from SSRFA front panel interface in local mode. In response to this signal (If DC_Inhibit and Safety Permit are OK), SSRFA initiates the turn-on process by switching ON contactors and then after some time (around 15 seconds) all amplifier power supplies will be turned on. After this, under no internal faults condition, SSRFA responds by SSA_Ready signal. This means that SSRFA is ready to accept RF input power from LLRF. This signal needs to be active high for around 200 ms to enable system ON/OFF to avoid false ON/OFF. This signal must be designed as hardwired on multi-pin (D-25) connector as command signal.

SSA_Inhibit: This signal breaks the RF connection from LLRF to the SSRFA via an RF switch (internal to SSRFA). High level TTL signal means OK and low level as fault. This is 50-Ohm fast TTL signal on a SMA (female) on Rear panel. This signal comes from RFPI and is used to switch OFF SSRFA when external fault is observed. An indication of inhibit is displayed on the front panel (HMI application).



Amplifier Interface Signals..

DC_Inhibit: A DC_Inhibit signal will be provided by the RFPI system. This is a TTL, 50 ohm to ground input and will be active HIGH, i.e. high indicates OK, low or disconnected cable means not OK. This signal will be available on SMA connector.

Safety Permit: A safety permit input will be a contact signal or equivalent. A closure indicates OK, while disconnected cable or open indicates NOT OK. This signal comes from the external safety interlock system. Conditions for this signal being open may be that the tunnel is not secured or other safety conditions are violated. If it is open, AC power to the SSRFA will be removed. This signal will be a dedicated input signal a potential free contact which is connected by 2 pin Phoenix Terminal Block connector.

Trigger/Gating signal: This signal comes from control system as a trigger for data acquisition. The actual data acquisition can be done relative to the rising edge of this pulse after a delay which is specified by the control system over Ethernet. The gate signal will be an active high 50 Ohm drive TTL signal. This timing gate comes from the accelerator timing/clock system and will synchronize the gating for pulsed operation. Nominal RF pulse width is 6 ms for PIP-II.

SSA_Alert: This is a soft warning signal, which indicates change in some state or that amplifier system is operating under some constraints (operating under de-rated mode of operation). Examples of warning conditions are water temperature above range or one RF modules in the amplifier is not healthy. This signal is communicated through Ethernet port to its HMI along with being indicated on local panel (with buzzer). This signal is communicated through Ethernet port to external control system also.

Amplifier Interface Signals

Reset: To reset SSRFA fault, after external/internal fault is removed. This signal needs to remain at high level for minimum of at least 200 ms for assertion of reset. Reset can also be performed from front panel in local mode. Reset can be performed via Ethernet port as well.

Pulse/CW Mode: It is input to SSRFA, giving information about operating mode (pulse/CW) of the amplifier.

Local/Remote Read Back: It is available on DB-25 as output from SSRFA, giving the information about Local or remote operating mode of the amplifier.

Control Interface Signal Details

1. **Fast TTL Control Input to RFPA**
2. **Slow Control Input to RFPA**
3. **TTL Status Outputs from the RFPA**
4. **Slow Status Output from the RFPA**
5. **Input and Output Signal Protection:** Inputs and outputs shall be protected against static discharge, over-voltage, and over-current conditions.
6. **Ethernet Port**: All the Amplifier operating point parameters, status signals will be made available to external systems via Ethernet port. Amplifier data can be read back and written to externally.

Signals to RFPI, External Control and Accelerator Safety Systems

Name	Signal Type	Connector	Cable	Polarity
SSA Inhibit	50Ω TTL	50Ω SMA	RG-58	Active Low
DC Inhibit	50Ω TTL	50Ω SMA	RG-58	Active Low
SSA Ready/Fault	50Ω TTL (50mA drive Max)	50Ω SMA	RG-58	Active High
Trigger/Gate	50Ω TTL	50Ω SMA	RG-58	Active High
Safety Permit	Active closed potential free relay contact (input)	2-pin Phoenix TB	2-wire twisted pair	

Name	Signal Type	Connector	I/O	Polarity	Min Hold Time
ON/OFF (start)	Opto-isolated 24V (20mA Max)	Standard D	Input	Active High	200 ms
SSA Reset	Opto-isolated 24V (20mA Max)	Standard D	Input	Active High	200 ms
SSA Ready/Fault	Optocoupler C-E (or D-S) pair (35V & 30mA Max)	Standard D	Output	High=Ready	
SSA Alert	Optocoupler C-E (or D-S) pair (35V & 30mA Max)	Standard D	Output	Active High	
Remote/Local	Optocoupler C-E (or D-S) pair (35V & 30mA Max)	Standard D	Output	High=Remote	
Pulse/CW	Opto-isolated 24V (20mA Max)	Standard D	Input	High=Pulse	

Relevant Publication List

[1]	Akhilesh Jain, D. K. Sharma, A. K. Gupta and M. Lad, "A 150 kW Pulse Solid State Amplifier for Radio Frequency Quadrupole Application," in *IEEE Transactions on Nuclear Science*, doi: 10.1109/TNS.2020.3025382, Sep 2020.
[2]	D. K. Sharma, Akhilesh Jain, K. Pathak and M. Lad, "Compact dual-channel radio frequency power sensor for solid state amplifiers," Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,, vol. 944, 2019.
[3]	Akhilesh Jain, A. K. Gupta, D. K. Sharma, P. R. Hannurkar and S. Pathak, "Design and analysis of a high-power radial multi-way combiner," International Journal of Microwave and Wireless Technologies, vol. 6, no. 1, pp. 83-91, 2014.
[4]	Akhilesh Jain, D. K. Sharma, A. K. Gupta, M. Lad, P. R. Hannurkar and S. K. Pathak, "System efficiency analysis for high power solid state radio frequency transmitter," Review of Scientific Instruments, vol. 65, no. 024707, pp. 1-8, 2014.
[5]	Akhilesh Jain, "Advanced harmonically tuned radio frequency power amplifiers," RRCAT Newsletter, vol. 31, no. 2, pp. 42-50, Dec 2018.
[6]	A. K. Gupta, Akhilesh Jain and M. Lad, "Design and development of 150 kW pulsed RF rigid coaxial line based 3-Way RF Power Combiner at 325 MHz," in Indian Particle Accelerator Conference, InPAC-19, New Delhi, 2019.
[7]	Akhilesh Jain, P. R. Hannurkar, D. K. Sharma, A. K. Gupta, A. K. Tiwari, R. Kumar, M. Lad, P. D. Gupta and S. K. Pathak, "Design and Characterization of 50 kW Solid-State RF Amplifier," International Journal of Microwave and Wireless Technologies, vol. 6, no. 1, pp. 83-91, 2012.

Thanks

FPGA Based Real Time Controller: Specifications

S.No.	Parameter	Value
1	Processor speed	667 MHz or higher
2	Operating system	Pre-installed Linux Real-Time OS
3	Nonvolatile Memory	512 MB or higher
4	System Memory	256 MB or higher
5	FPGA flip flops	1,00,000 (min.)
6	FPGA block RAM	4 MB (min.)
7	No. of DMA channels	8 (min.)
8	Network interface	100/1000 Mbps Ethernet
9	Serial communication	RS-232 with baud rate 115200 bits/second
10	USB device port	USB 2.0 or better
11	USB host port	USB 2.0 or better
12	Programmability	Programmable and configurable with LabVIEW software
13	Compatibility	Full compatibility with NI 9205 series Analog and Digital I/O modules
14	Chassis	Integrated 8 slots chassis
15	I/O module slots	8 DB-15 connector on chassis for I/O modules
16	Chassis integrations	Integrated Real Time controller and FPGA backplane connected to I/O